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STRAINED SEMICONDUCTOR BY FULL WAFER BONDING

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Cross Reference To Related Applications

This application is related to the following commonly assigned U.S. patent applications which are herein incorporated by reference in their entirety: "Cellular Materials Formed Using Surface Transformation," U.S. Application Serial Number 10/382,246, filed on March 5, 2003;"Micro-Mechanically Strained Semiconductor Film," U.S. Application Serial Number 10/379,749, filed on March 5, 2003; "Localized Strained Semiconductor On Insulator," U.S. Application Serial Number 10/425,797, filed on April 29, 2003; "Strained Si/SiGe Structures by Ion Implantation," U.S. Application Serial Number 10/431,134, filed on May 7, 2003; "Strained Semiconductor by Wafer Bonding with Misorientation," U.S. Application Serial Number 10/425,484, filed on April 29, 2003; "Micromechanical Strained Semiconductor By Wafer Bonding," U.S. Application Serial Number 10/431,137, filed on May 7, 2003; and "Strained Si/SiGe/SOI Islands and Processes of Making Same," U.S. Application Serial Number _______, filed on ________ (Attorney Docket 1303.102).

Technical Field

This disclosure relates generally to integrated circuits, and more particularly, to strained semiconductor structures.

Background

The semiconductor industry continues to strive for improvements in the speed and performance of semiconductor devices. Strained silicon technology enhances carrier mobility in both n-channel and p-channel devices, and thus improves device speed and performance.

One technique for producing strained silicon involves growing silicon on relaxed silicon germanium (Si/SiGe) structures. There is a large mismatch in the cell structure between the Si and SiGe layers. This mismatch causes a pseudomorphic layer of Si on relaxed SiGe to be under a tensile strain that modifies the band structure and enhances carrier transport in the Si layer. In an electron inversion layer, the subband splitting is larger in strained Si because of the strain-induced band splitting in addition to that provided by quantum confinement. For example, the ground level splitting ($E_0(d_4)$ - $E_0(d_2)$) in a MOS inversion layer at 1 MV/cm transverse field is ~120 meV for unstrained Si and ~250 meV for strained Si. The increase in energy splitting reduces inter-valley scattering and enhances NMOSFET mobility, as demonstrated at low (<0.6 MV/cm) and higher (~ 1MV/cm) vertical fields. The scaled transconductance (g_m) is also improved due to the reduced density of states and enhanced non-equilibrium transport.

One method for forming the Si/SiGe layer involves epitaxially growing the Si and SiGe layers using an ultra-high vacuum chemical vapor deposition (UHVCVD) process. The UHVCVD process is a costly and complex process. The Ge content is graded in steps to form a fully relaxed SiGe buffer layer before a thin (~20 nm) strained Si channel layer is grown. X-ray diffraction analysis can be used to quantify the Ge content and strain relaxation in the SiGe layer. The strain state of the Si channel layer can be confirmed by Raman spectroscopy. One proposed back end approach for straining silicon applies uniaxial strain to wafers/dies after the integrated circuit process is complete. The dies are thinned to membrane dimensions and then affixed to curved substrates to apply an in-plane, tensile strain after device manufacture.

There is a need in the art to provide improved strained semiconductor films and devices that incorporate the strained films, and to provide improved methods for forming strained semiconductor films.

Summary

The above mentioned problems are addressed and will be understood by reading and studying this specification. Various aspects and embodiments of the present invention mechanically stretch a semiconductor layer during full wafer bonding to form a wafer with a strained semiconductor layer. According to various embodiments, the strained semiconductor layer is an ultra-thin silicon layer.

One aspect of this disclosure relates to a method for forming a wafer. In various embodiments of the method, a predetermined contour is formed in one of a semiconductor membrane and a substrate wafer. The semiconductor membrane is bonded to the substrate wafer and the predetermined contour is straightened to induce a predetermined strain in the semiconductor membrane. In various embodiments, a substrate wafer is flexed into a flexed position, a portion of the substrate wafer is bonded to a semiconductor layer when the substrate wafer is in the flexed position, and the substrate wafer is relaxed to induce a predetermined strain in the semiconductor layer. In various embodiments, a central region of a substrate wafer is flexed into a flexed position, a bond cut process is performed to form a silicon membrane from a crystalline sacrificial wafer and bond a peripheral region of the substrate wafer to a peripheral region of a silicon membrane when the substrate wafer is in the flexed position, and the substrate wafer is relaxed to induce a predetermined strain in the silicon membrane. Other aspects and embodiments are provided herein.

This Summary is an overview of some of the teachings of the present application and not intended to be an exclusive or exhaustive treatment of the present subject matter. Further details are found in the detailed description and appended claims. Other aspects will be apparent to persons skilled in the art upon reading and understanding the following detailed description and viewing the drawings that form a part thereof, each of which are not to be taken in a limiting sense. The scope of the present invention is defined by the appended claims and

their legal equivalents.

Brief Description of the Drawings

Figure 1 illustrates the lattice constant of a $Si_{1-X}Ge_X$ substrate for different percentages (X) of Ge.

Figure 2 illustrates the mobility enhancement for strained Si for different percentages (X) of Ge in a $Si_{1-X}Ge_X$ substrate.

Figure 3 illustrates a relationship between elastic strain and semiconductor layer thicknesses.

Figures 4A-4B illustrate a wafer and a full wafer bonding process, respectively.

Figures 5A-5D illustrate a process for straining a semiconductor layer by performing a bond-cut process to bond the semiconductor layer to a flexed bow-shaped substrate, according to various embodiments of the present invention.

Figures 6A-6B illustrate relaxed and flexed wafer positions, and a strain for a wafer in the flexed position.

Figures 7A-7B illustrate a stress calculation for a bowed substrate wafer.

Figure 8 illustrates a composite structure that includes a strained semiconductor membrane bonded to a flexible substrate, and further illustrates the composite structure being bonded to a thicker carrier substrate, according to various embodiments of the present invention.

Figures 9A-9B illustrate a process for straining a semiconductor layer by performing a bond-cut process to a bowed substrate with voids, according to various embodiments of the present invention.

Figure 10A-10F illustrate a process to form a wafer with a sphere-shaped empty space, according to various embodiments of the present invention.

Figure 11A-11C illustrate a process to form a wafer with a pipe-shaped empty space, according to various embodiments of the present invention.

Figures 12A-12B illustrate a process to form a wafer with a plate-shaped empty space, according to various embodiments of the present invention.

Figure 13A-13E illustrate the formation of empty spheres from initial cylindrical holes in a wafer with the same radii and with varying length, according to various embodiments of the present invention.

Figure 14 illustrates a wafer with a surface-transformation-formed stack of empty plates with a large filling factor or low density, according to various embodiments of the present invention.

Figures 15A-15C illustrate a process for straining a semiconductor layer by performing a bond-cut process to bond a relaxed bow-shaped semiconductor layer to and flatten the semiconductor layer against a rigid substrate, according to various embodiments of the present invention.

Figures 16A-16D illustrate a process for straining a semiconductor layer by bonding a concave surface of a crystalline wafer to a rigid substrate, according to various embodiments of the present invention.

Figure 17 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the present invention.

Figure 18 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17.

Figure 19 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17.

Figure 20 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17.

Figure 21 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17.

Figure 22 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17.

Figure 23 illustrates a transistor fabricated with a strained semiconductor membrane, according to various embodiments of the present invention.

Figure 24 illustrates a simplified block diagram of a high-level organization of a memory device, according to various embodiments of the present invention.

Figure 25 illustrates a simplified block diagram of a high-level organization of an electronic system according to various embodiments of the present invention.

Detailed Description

The following detailed description refers to the accompanying drawings which show, by way of illustration, specific aspects and embodiments in which the present invention may be practiced. References to "an", "one", or "various" embodiments in this disclosure are not necessarily to the same embodiment, and such references contemplate more than one embodiment. The various embodiments are not necessarily mutually exclusive as aspects of one embodiment can be combined with aspects of another embodiment. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. In the following description, the terms wafer and substrate are interchangeably used to refer generally to any structure on which integrated circuits are formed, and also to such structures during various stages of integrated circuit fabrication. Both terms include doped and undoped semiconductors, epitaxial layers of a semiconductor on a supporting semiconductor or insulating material, combinations of such layers, as well as other such structures

that are known in the art. The terms "horizontal" and "vertical", as well as prepositions such as "on", "over" and "under" are used in relation to the conventional plane or surface of a wafer or substrate, regardless of the orientation of the wafer or substrate. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims, along with the full scope of equivalents to which such claims are entitled.

Aspects of the present invention strain a semiconductor layer, such as a crystalline silicon layer, by mechanical stretching of the semiconductor layer during full wafer bonding. In various embodiments, the semiconductor layer is an ultra-thin semiconductor layer. Various embodiments bond the ultra-thin semiconductor layer to a bowed flexible substrate during full wafer bonding. Various embodiments bond a semiconductor layer with a bowed surface to a fixed wafer during a full wafer bonding.

This detailed description is organized as follows. First, this discussion uses research findings of Si/SiGe to determine a desired mechanical strain for the semiconductor layer. Second, a brief discussion of full wafer bonding is provided. Third embodiments that bond semiconductor membranes to a bowed, flexible substrate are discussed. Various embodiments bow a thin flexible substrate, and various embodiments bow a thicker flexible substrate having voids formed by surface transformation. Fourth, this disclosure discusses bonding relaxed ultra-thin semiconductor membrane with a bowed shape to a rigid substrate. Fifth, this disclosure discusses bonding a single crystal wafer with a relaxed concave surface to a rigid substrate. Sixth, this disclosure discusses various method aspects for straining a semiconductor layer at a wafer scale. Seventh, this disclosure discusses a transistor that incorporates the strained semiconductor. Eighth, this disclosure discusses systems such as memory devices and computers. The headings and numbering used to organize the detailed description should not be used to limit the

present invention, but rather are intended to assist the reader in navigating through this disclosure.

1. Desired Mechanical Strain

This disclosure discusses mechanically straining a wafer-sized semiconductor layer, *i.e.* straining a semiconductor layer at a wafer scale. According to embodiments provided in this disclosure, silicon is mechanically strained to enhance carrier mobility. Other semiconductor material can be strained in accordance with the subject matter discussed herein. Research findings for Si/SiGe structures can be used to determine desirable mechanical strain.

Si has a lattice constant of 5.43095 Å, and Ge has a lattice constant of 5.64613 Å. The lattice constant of SiGe is between the lattice constant of Si and the lattice constant of Ge, and depends on the percentage of Ge in the SiGe layer. Figure 1 illustrates the lattice constant of a $Si_{1-X}Ge_X$ substrate for different percentages (X) of Ge. As indicated by Figure 1, a $Si_{1-X}Ge_X$ substrate containing about 30% Ge ($X \approx 0.3$) has a lattice constant of about 5.50 Å. The biaxial strain of the Si on the SiGe can be calculated as follows:

$$(1) \qquad Biaxial\_Strain = \frac{SiGe_{LC} - Si_{LC}}{Si_{LC}}$$

where the subscript LC represents the lattice constant of the SiGe or Si. Thus, as shown in Equation 2, the Si on the SiGe substrate has a biaxial strain of about 1.28%.

$$(2) \qquad Biaxial\_Strain \approx \frac{5.50 - 5.43}{5.43} = 1.28\%.$$

Figure 2 illustrates the mobility enhancement for strained Si for different percentages (X) of Ge in a $Si_{1-X}Ge_X$ substrate. The mobility enhancement increases as the percentage of Ge in the $Si_{1-X}Ge_X$ increases, and levels off to around 1.6 when

the percentage of Ge is around 22% or larger. Referring to Figure 1, 22% Ge provides the $Si_{1-X}Ge_X$ substrate with a lattice constant ($SiGe_{LC}$) of around 5.485. Using Equation 1, it is determined that the corresponding strain for 22% Ge (the approximate point where the mobility enhancement levels off) is about 1%.

When the percentage of Ge in the $Si_{1-X}Ge_X$ is about 20% (near the knee of the curve), it can be calculated that the resulting strain is about 0.75%. When the percentage of Ge in the $Si_{1-X}Ge_X$ is about 40%, it can be calculated that the resulting strain is about 1.5%. Referring again to Figure 1, it can be seen that a $Si_{1-X}Ge_X$ substrate having just under 10% Ge still provides considerable mobility enhancement (1.3). A $Si_{1-X}Ge_X$ substrate having just under 10% Ge provides the $Si_{1-X}Ge_X$ substrate with a lattice constant ($SiGe_{LC}$) of around 5.457. Using Equation 1, it is determined that the corresponding strain is around 0.5%. Thus, it is desirable to achieve a biaxial strain around or greater than 0.5%, and preferably around 1% or greater to obtain the desired enhanced mobility associated with strained Si.

Various embodiments of the present invention mechanically induce a strain in thin semiconductor wafers. Figure 3 illustrates a relationship between elastic strain and semiconductor layer thicknesses. The semiconductor yield is plotted with respect to plastic deformation and defects in bulk samples. The illustrated values represent the relationship of thin SiGe layers on silicon. Figure 3 illustrates that thin layers of silicon or other semiconductor materials are more tolerant of strain than thick bulk samples. Previously, thin layers of SiGe have been fabricated on silicon because of the tolerance of the thin layers to strain. Figure 3 indicates that 1000 Å thin semiconductor layers can be strained up to about 1%, that 100 Å thin semiconductor layers can be strained up to about 2% and thinner semiconductor layers can be strained up to about 2.5%. However, as illustrated earlier with respect to Figure 2, the mobility enhancement levels off when the strain reaches about 1%.

It is thus desirable to strain a thin semiconductor layer, such as a silicon layer, with a strain greater than 0.5% to achieve significant mobility enhancement.

For further mobility enhancement, it is desirable to strain a thin semiconductor wafer, such as an ultra-thin silicon wafer with a thickness within a range of approximately 300 Å to 1000 Å, with a strain within a range of approximately 0.75% to approximately 1.5% where the mobility enhancement levels off. It is also desirable to reduce unnecessary strain and provide a margin for error without unduly affecting the mobility enhancement. Thus, it is desirable to strain a thin semiconductor layer, such as a thin silicon layer, with a strain in the range of approximately 1% to approximately 1.2%.

Ultra-thin wafers, such as single crystalline silicon wafers, have a thickness below approximately 200 microns, which is near the limit of known mechanical thinning techniques. Virginia Semiconductor, Inc. has produced these wafers with a thickness down to about 2 microns with diameters of up to 4 inches. Doping concentrations and profiles for these wafers are comparable to normal thickness wafers, and the Total Thickness Variation (TTV) is generally less than one micron. Bond-quality, ultra-thin wafers are double side polished and have micro-roughness comparable to prime grade, normal thickness wafers. Ultra-thin wafers that have a thickness of approximately 100 microns or more are mechanically similar to normal wafers and can be processed using standard techniques. As the thickness decreases further, the wafer exhibits greater flexibility to the point, at about 20 microns thick, that the wafer can be deformed into a tube, with the wafer contacted flat with the opposite edge. At a thickness less than about 10 microns, ultra-thin wafers become transparent to visible light. The increased flexibility allows ultra-thin wafers to bond to surfaces with roughness orders of magnitude greater than the limit for bonding normal thicknesses.

Recently, a bond cut technique, referred to in literature as a Smart-Cut technique, has been described for producing silicon on insulator wafers for integrated circuits. As will be described in detail below, the bond cut technique implants ions such as hydrogen, bonds two wafer surfaces together, and separates

the two bonded wafers along the region of hydrogen implantation. The literature indicates that memory structures have been inverted and stacked capacitors have been buried by wafer bonding. Various techniques such as grinding, polishing, chemical etch, chemical etch with etch stops, and/or plasma assisted chemical etch, can be used to further thin the top wafer to a thickness on the order of a micron after the wafers are bonded. Besides oxide or silicon, silicon has been bonded on other materials such as sapphire wafers.

The bond cut technique will be discussed in further detail in the section entitled "Bonding Semiconductor Membrane to Bowed Substrates." In various embodiments, the ultra-thin semiconductor film is produced by a hydrogen implantation into a sacrificial wafer leaving a single crystalline 300 Å to 1000 Å surface layer which will separate from the carrier wafer when the film is bonded face down on the device wafer. After the final high temperature bonding heat treatment, the bonded layer is polished by chemical and/or mechanical means to make the surface smoother leaving an ultra-thin strained film on the order of 300 Å to 1000 Å thick.

2. *Full Wafer Bonding*

Figures 4A-4B illustrate a wafer and a full wafer bonding process, respectively. Various techniques to produce strained semiconductor involve a full wafer bonding technique. Various embodiments produce strained silicon layers on silicon, glass, quartz, silicon oxycarbide and other glass substrates.

Figure 4A illustrates a wafer 401. A common wafer size is 8 inches in diameter. However, wafers are capable of being fabricated in other sizes. The present invention is not limited to wafers of a particular size. A number of dies can be formed on a wafer. A die 402 is an individual pattern, typically rectangular, on a substrate that contains circuitry to perform a specific function. A semiconductor wafer typically contains a repeated pattern of such dies containing the same

functionality. A die is typically packaged in a protective casing (not shown) with leads extending therefrom (not shown) providing access to the circuitry of the die for unilateral or bilateral communication and control.

Figure 4B generally illustrates full wafer bonding process. A wafer-sized membrane 403 is bonded to a wafer substrate 404 such that the substrate wafer, or at least as portion of the substrate wafer, is covered by the membrane. The wafer-sized membrane need not be exactly the same size as the wafer. The term "wafer-sized" reflects that the bonding of the membrane to the wafer occurs on a wafer scale. The wafer substrate 404 generally corresponds to the wafer 401 illustrated in Figure 4A without dies. The circuitry is formed in the bonded membrane after the full wafer bonding process. Various techniques and mechanisms can be used to perform a full wafer bonding process.

3. Bonding Semiconductor Membrane to Bowed Substrates

Figures 5A - 5D illustrate a process for straining a semiconductor layer by performing a bond-cut process to bond the semiconductor layer to a flexed bow-shaped substrate, according to various embodiments of the present invention. The bond cut process involves bonding together two substrates, or wafers, and breaking off a section (*i.e.* the membrane) of at least one of the two substrate after the substrates have been bonded together. The substrate is also referred to herein in various embodiments as a flexible wafer or substrate wafer. The membrane is broken off of a second wafer or sacrificial wafer.

Figure 5A illustrates a sacrificial semiconductor wafer 505, and Figure 5B illustrates a substrate wafer 504. In various embodiments, the substrate wafer 504 includes one of the following materials: silicon; germanium; silicon–germanium; gallium arsenide; indium phosphide; and other semiconductor materials. In various embodiments, the substrate wafer 504 includes glass, quartz, silicon oxycarbide, and other glass substrates. This list of materials is not intended to be an all-inclusive

list. In various embodiments, the sacrificial wafer includes various semiconductor material including but not limited to silicon, germanium, silicon–germanium, gallium arsenide, indium phosphide. The sacrificial wafer 505 can include other semiconductor materials.

The sacrificial wafer 505 is a single crystal wafer. The bond-cut technique conditions the sacrificial wafer 505 by implanting ions 506 into a surface 507. The ions are implanted along a plane, represented in Figure 5A as a dotted line 508, to define a semiconductor membrane 503 with a predetermined thickness. The plane 508 is approximately parallel to the surface 507 in which the ions 506 are implanted. In various embodiments, hydrogen ions are used as implantation ions. In various embodiments, the hydrogen ions include H^+, H_2^+, D^+, and/or D_2^+ ions. The implanted ions act to form cavities along the plane 508. The cavities are joined through thermal processing, allowing the membrane 503 to be removed from the remaining portion of the sacrificial wafer 509 at the cleavage plane 508. In various embodiments, this thermal processing occurs while the membrane 503 is being bonded to the substrate wafer 504, as shown in Figure 5C. Once these cavities join and the surface layer is bonded to the substrate, the surface layer breaks off of the sacrificial wafer at the cleavage plane and remains bonded to the substrate. The remaining portion of the sacrificial wafer 505 can be used to form membranes for other substrates, thus reducing waste and the overall cost for the manufacturing process for a wide variety of electronic devices.

In the illustrated embodiment, the periphery of the substrate wafer 504 is supported by a vacuum chuck 510. The substrate wafer 504 is flexible and is capable of being influenced into a flexed position. In the illustrated embodiment, a vacuum or near vacuum, represented by arrows 511, draws the substrate wafer 504 into the chuck 510.

Figure 5C illustrates the surface layer 507 of the sacrificial wafer 505 bonded to portions of the substrate wafer 504. In various embodiments, the periphery of the

membrane 503 is bonded to the periphery of the substrate wafer 504. The periphery of the membrane and the periphery of the flexible substrate wafer are initially bonded together when the flexible substrate wafer is bowed. In the illustrated embodiment, the membrane 503 is bonded in a vacuum environment to the edge portions of the bowed substrate wafer 504. This vacuum, or near vacuum, draws the flexible substrate wafer into a contour shape (e.g. a bow). In various embodiments, this bonding is accomplished at a low temperatures in the order of 300° C to 400° C.

In various embodiments, the bonded wafers are heated to further bond the membrane 503 to the substrate wafer 504 and to cut the membrane 503 from the sacrificial wafer 505. In various embodiments, the bonding temperature is within a range of approximately 300° C to 400° C. Heating the sacrificial wafer joins the cavities in the cleavage plane 508, allowing the remaining portion 509 of the sacrificial wafer to be removed from the membrane 503, which remains bonded to the substrate wafer 504. The remaining portion 509 of the sacrificial wafer 505 can be prepared and conditioned for another bond-cut process.

In Figure 5D, the substrate wafer 504 is subjected to atmospheric pressure, and is removed from the vacuum chuck, which causes the flexible substrate wafer 504 to straighten (*i.e.* relax from its bow shape to a straight or relatively straight shape). The substrate wafer 504 induces a strain (represented by arrows 511) in the membrane 503 when the bowed contour is removed from the substrate, *i.e.* when the substrate wafer 504 relaxes from a flexed (bowed) position. A final wafer bonding is completed at a higher temperature in the order of 800° C to 100° C. Before the surface layer is bonded to the substrate, the sacrificial wafer and the substrate can be cleaned using conventional cleaning procedures. In various embodiments, the bonding force includes the strong Van der Waal's force that naturally bonds surfaces together as the bonding force. In various embodiments, the Van der Waal's force provides an initial bonding force that is strengthened during subsequent thermal

processing.

The thickness of the membrane 503 bonded to the substrate wafer 504 is defined by the depth of ion implantation during the bond-cut process. In various embodiments, the thickness of the membrane 503 is such that it does not yield or otherwise plastically deform under the desired mechanical strain induced by the bond. In various embodiments, the thickness of the membrane 503 is less than 200 nm, and as such is termed an ultra thin wafer. In various embodiments, the silicon layer has a thickness of about 0.1 microns (100 nm or 1000 Å). In various embodiments, the silicon layer has a thickness less than 0.1 microns. In various embodiments, the silicon layer has a thickness in a range of approximately 300 Å to 1000 Å.

In various embodiments, the silicon film is prepared for transistor fabrication. A transistor structure is discussed with respect to Figure 23. In various embodiments, the preparation of the film includes grinding, polishing, chemical etch, chemical etch with etch stops, and/or plasma assisted chemical etch, and the like, which can be used to further thin the film. Thus, the membrane bonded to the substrate illustrated in Figure 5D can be thinner than the surface layer defined in the sacrificial layer in Figure 5A. Device processing can be accomplished using conventional processes and procedures.

Figures 6A-6B illustrate relaxed and flexed wafer positions, and a strain for the wafer in the flexed position. In Figure 6A, the solid line represents a profile of the wafer substrate 604 in a straight or relaxed state, and the dotted line represents a profiled of the wafer substrate influenced or flexed into a flexed state. A strain is induced in the wafer substrate when influenced into the flexed state.

Figure 6B illustrates the strain in the bowed substrate. The illustrated wafer substrate 604 is bowed prior to bonding parts of the membrane to the substrate (e.g. bonding the periphery of the membrane to the periphery of the substrate). In various embodiments, the semiconductor membrane is an ultra-thin single crystalline

silicon layer. In various embodiments, the semiconductor layer has a thickness within a range of approximately 300 Å to 1000 Å. In various embodiments, the semiconductor layer has a thickness (T) of about 300 Å (30 nm) suitable for use to form a transistor channel less than or equal to about 1000 Å (100 nm). The process according to various embodiments of the present invention can be geometrically represented using a triangle with a first leg 612 representing half the diameter of the wafer, and a second leg 613 representing the depth of the bow. The hypotenuse 614 of the triangle represents the strain in the bowed substrate. The strain of the substrate is transferred to the membrane when the bowed substrate is relaxed. As is shown with respect to this figure, a 1% strain can be achieved by bowing an 8 inch diameter substrate by about one half inch. An 8 inch wafer has a radius of 4 inches (or approximately 100 mm), which is represented in a relaxed state as the horizontal leg 612 of the triangle. Straining the wafer substrate by 1% increases the length from 100 mm to 101 mm, which is represented by the hypotenuse 614 of the triangle. The vertical leg 613 of the triangle represents a distance traveled when a substrate wafer is bowed into a flexed position. This distance can be determined using the following equations.

$$\begin{aligned} &(100^2)+d^2=(101)^2; \\ &d^2=201; \\ &d\approx 14mm \approx 560mils \approx \frac{1}{2}inch. \end{aligned} \tag{3}$$

As stated earlier with respect to Si/SiGe layers, it is desired to provide silicon with a strain around or greater than 0.5% to obtain the desired enhanced mobility associated with strained silicon. Thus, as shown by the example illustrated in Figures 5A-5D, various embodiments of the present invention are capable of providing strains in this range. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to bow the substrate, bond a membrane to the bowed substrate, and relax the substrate to provide the membrane

with a desired strain. In various embodiments, the substrate is bowed to an extent such that, after bonding the semiconductor membrane and the relaxing the bow in the substrate, the substrate induces a strain in the semiconductor membrane greater than 0.5%. In various embodiments, the substrate is bowed to an extent such that, after bonding the semiconductor membrane and the relaxing the bow in the substrate, the substrate induces a strain in the semiconductor membrane between approximately 0.75% to approximately 1.5%. In various embodiments, the substrate is bowed to an extent such that, after bonding the semiconductor membrane and the relaxing the bow in the substrate, the substrate induces a strain in the semiconductor membrane between approximately 1% to approximately 1.2 %.

Figures 7A-7B illustrate a stress calculation for a bowed substrate wafer. The mechanical force, F_m, required to mechanically cause a deflection (D) is:

(4) $$F_m = \frac{4Et^3 D}{x^2 - y^2},$$

where E is Youngs modulus in N/mm^2, t is the thickness of the wafer in mm, D is the deflection in mm, and x and y are dimensions represented in the figure. The maximum bending stress (σ_{max}) in N/mm^2 is:

(5) $$\sigma_{max} = \frac{3F}{2t^2},$$

where F is the mechanical force.

The literature shows that a 100 μm (approximately 4 mil or 4/1000 inch) silicon substrate is very flexible and will easily bow. A glass substrate has similar characteristics. Flexible substrates are typically thin. However, thicker substrates are desirable for some applications. Two approaches with respect to the competing demands of a thicker substrate and a flexible substrate are provided below. In one approach, a semiconductor membrane is bonded to a thin flexible substrate such as illustrated in Figures 5A-5D, and the resulting composite structure is bonded to a thicker carrier substrate. In the second approach, a semiconductor membrane is

bonded to a thicker substrate that includes voids to provide the thicker substrate with flexibility.

Bonding to Thin Flexible Substrate,
and Bonding Composite to Thicker Carrier Substrate

Figure 8 illustrates a composite structure that includes a strained semiconductor membrane bonded to a flexible substrate, and further illustrates the composite structure being bonded to a thicker carrier substrate, according to various embodiments of the present invention. In the illustration, the composite structure 815 includes a strained semiconductor membrane 803 and a flexible substrate wafer 804, which in various embodiments is fabricated according the process illustrated and discussed with respect to Figures 5A-5D. The composite structure 815 is bonded (represented by arrows 816) to a thicker carrier substrate 817. In various embodiments, the thicker carrier substrate 817 includes glass, quartz, a silicon oxycarbide glass, aluminum oxycarbide glass, or silicon.

Bonding Directly to Flexible Substrate Formed with Surface Transformed Voids

Figures 9A-9B illustrate a process for straining a semiconductor layer by performing a bond-cut process to a bowed substrate with voids, according to various embodiments of the present invention. The voids, such as nano-voids, modifies Young's modulus for the thicker substrate, and cause the thicker substrate wafer to be flexible. Voids in silicon or glass can be realized by a surface transformation process, where holes are etched into the material and then the material is annealed below its melting temperature. Surface transformation is discussed in "Cellular Materials Formed Using Surface Transformation," U.S. Application Serial Number 10/382,246, filed on March 5, 2003, which has previously been incorporated by reference. Using the surface transformation technique, the voids can be precisely formed with a desired shape and size in a desired position. Various embodiments

incorporate voids into various substrate types, including but not limited to glass and silicon substrates. Materials with voids can be referred to as cellular material.

Figure 9A illustrates a bond-cut technique performed to bond a membrane 903, such as an ultra-thin silicon layer, to a flexible substrate 919 with voids 920. Figure 9A also illustrates the surface layer 907 of the sacrificial wafer 905 bonded to portions of the substrate wafer 919. In various embodiments, the periphery of the membrane 903 is bonded to the periphery of the substrate wafer 919. The periphery of the membrane and the periphery of the flexible substrate wafer are initially bonded together when the flexible substrate wafer 919 is bowed. In the illustrated embodiment, the membrane 903 is bonded in a vacuum environment to the edge portions of the bowed substrate wafer 919. This vacuum, or near vacuum, draws the flexible substrate wafer into a contour shape (e.g. a bow). In various embodiments, this bonding is accomplished at a low temperatures in the order of 300° C to 400° C.

The bonded wafers can be heated to further bond the membrane 903 to the substrate wafer 919 and to cut the membrane 903 from the sacrificial wafer 905. In various embodiments, the bonding temperature is within a range of approximately 300° C to 400° C. Heating the sacrificial wafer joins the cavities in the cleavage plane 908, allowing the remaining portion 909 of the sacrificial wafer to be removed from the membrane 903, which remains bonded to the substrate wafer 919. The remaining portion 909 of the sacrificial wafer 905 can be prepared and conditioned for another bond-cut process.

With reference to Figure 9B, the substrate wafer 919 is subjected to atmospheric pressure, and is removed from the vacuum chuck 910, which causes the flexible substrate wafer 919 to straighten (*i.e.* relax from its bow shape to a straight or relatively straight shape). The substrate wafer 919 induces a strain (represented by arrows 911) in the membrane 903 when the bowed contour is removed from the substrate, *i.e.* when the substrate wafer 919 relaxes from a flexed (bowed) position. A final wafer bonding is completed at a higher temperature in the order of 800° C to

1000° C. Before the surface layer is bonded to the substrate, the sacrificial wafer and the substrate can be cleaned using conventional cleaning procedures. In various embodiments, the bonding force includes the strong Van der Waal's force that naturally bonds surfaces together as the bonding force. In various embodiments, the Van der Waal's force provides an initial bonding force that is strengthened during subsequent thermal processing.

Cellular materials provide interesting combinations of physical and mechanical properties. The substrate is referred to in this discussion as a flat panel.

The relationship between the stiffness (*S*) of a flat panel, the Young's modulus (*E*) of the panel material (representing the ability of the panel material to resist elastic strain), and the thickness (*h*) of the panel can be represented by:

(6) $$S \propto E \times h^3.$$

Cellular material that has imperfections such as the lack of uniformity and closure of the voids can be characterized by the following experimentally-found exponential relationship between the Young's modulus (*E*) and density (ρ).

(7) $$E \propto \rho^2.$$

Substituting Equation No. 7 for *E* in Equation No. 6 results in Equation No. 8.

(8) $$S \propto \rho^2 \times h^3.$$

The following observations can be made for panels constructed of imperfect cellular material (*i.e.* material with nonuniform voids and/or lack of closure of voids). For a panel of a given footprint area and height, constructing the panel using imperfect cellular material half as dense ($\rho/2$) results in a panel that one fourth as stiff (*S/4*). Thus, imperfect cellular material provides certain benefits related to flexibility.

A perfect cellular material with uniform and closed voids is expected to provide a linear relationship between the Young's modulus (E) and the density (ρ), as represented by Equation No. 9.

(9) $$E \propto \rho.$$

Substituting Equation No. 9 for E in Equation No.6 results in Equation No. 10.

(10) $$S \propto \rho \times h^3.$$

The following observation can be made for panels constructed of material that approaches a perfect or ideal cellular material (material with uniform voids and closure of voids). For a panel of a given footprint area and height, constructing the panel using perfect cellular material half as dense ($\rho/2$) is expected to result in a panel that is half as stiff ($S/2$).

Various embodiments provide a flexible material with a precisely-determined arrangement of voids (also referred to herein as empty spaces) using a surface transformation process. The substrate in which the voids are formed has a well-defined melting temperature. The substrate is annealed in a temperature range below and near the melting temperature to transform a predetermined arrangement of holes through a surface of the substrate into the desired predetermined arrangement of voids. The substrate is capable of being engineered for various structural and mechanical applications.

The uniformity, density, and space symmetry of the substrate is precisely determined by controlling the diameter, depth and position of an initial arrangement of cylindrical holes formed through a surface of a solid. In various embodiments, the holes have a generally-elongated shape extending into the volume away from the surface. In various embodiments, the holes have a generally cylindrical shape. The present subject matter is not so limited, however. In various embodiments, the precisely-controlled position of the voids is designed to provide a perfect cellular material, an imperfect cellular material, or somewhere between a perfect and imperfect cellular material such that the stiffness is between that provided in Equations 8 and 10. In various embodiments, the precisely-determined arrangement of voids provides the cellular material with an anisotropic stiffness.

When a solid is heated to a higher temperature, a solid with a hole that is beyond a critical length (λ_c) becomes unstable. For the purposes of the analysis provided below and to simplify the disclosure, the holes are referred to as cylindrical holes. However, various embodiments perform a surface transformation process using holes that are not geometrically cylindrical.

The cylindrical hole is transformed into one or more empty spheres formed along the cylinder axis. The number (N) of spheres formed depends on the length (L) and radius (R_C) of the cylinder. Two models of diffusion are the surface diffusion model and the pure volume diffusion model. With respect to the surface diffusion model, for example, the relation between the cylinder length (L), cylinder radius (R_C), and number of spheres (N) is expressed by the following equation:

$$(11) \quad 8.89 \times R_C \times N \leq L < 8.89 \times R_C \times (N+1).$$

Equation 11 predicts that no empty spheres will form if $L < 8.89 \text{ x } R_C$. Each empty sphere that forms has a radius (R_S) expressed by the following equation:

$$(12) \quad R_S = 1.88 \times R_C.$$

If the cylinder has sufficient length L to form two spheres, the center-to-center spacing between the spheres corresponds to the critical length (λ_C) and is provided by the equation:

$$(13) \quad \lambda_C = 8.89 \times R_C.$$

The pure volume diffusion model provides similar results, with slightly different constants. For example, depending on the exact magnitude of the diffusion parameters, λ_C can vary from $9.02 \text{ x } R_C$ to $12.96 \text{ x } R_C$. The diffusion model is capable of being determined by experiment. The remainder of this disclosure uses the surface diffusion model. One of ordinary skill in the art will understand, upon reading and comprehending this disclosure, how to apply this disclosure to another diffusion model.

Various shaped empty spaces or voids such as sphere-shaped voids, pipe-

shaped voids, and plate-shaped voids are capable of being formed under the surface of a substrate with a well-defined melting temperature. The shape of the empty spaces formed during the annealing conditions depends on the size, number and spacing of the cylindrical holes that are initially formed at a lower temperature.

Various predetermined arrangements of empty spaces or voids are capable of being formed under the surface of a substrate with a well-defined melting temperature. For example, an appropriately-sized deep trench in a material with a well-defined melting temperature is transformed into empty spheres along the axis of the original trench at an annealing temperature within a predetermined a range below the melting temperature. The empty spheres are uniformly sized and spaced. Other predetermined arrangements are provided below.

Figures 10A-10F illustrate a process to form a wafer with a sphere-shaped empty space, according to various embodiments of the present subject matter. A cylindrical hole 1021 is formed through the surface 1022 of a substrate 1019. As used here, the term hole refers to a void that extends from a surface of the volume into the solid material and that is defined by the solid material. The material is heated (annealed) and undergoes the transformation illustrated in Figures 10B through 10F. The desired annealing temperature is dependent on the well-defined melting temperature of the substrate. The result of the surface transformation process is an empty sphere formed below the surface 112 of the substrate.

In order to form a single sphere, which holds true for forming a single pipe (Figures 11A - 11C) or plate (Figures 12A - 12B), the length (L) and radius (R_C) of the cylindrical holes are chosen such that Equation No. 11 with N = 1 is satisfied. A vertical stacking of N empty spaces results if the length of the cylindrical holes is such that Equation No. 11 is satisfied.

In order for single surface-transformed spheres to combine with other surface-transformed spheres, the center-to-center spacing (D_{NT}) between the initial cylindrical holes will satisfy the following equation:

(14) $2 \times R_C < D_{NT} < 3.76 \times R_C$.

Satisfying this equation prevents the adjacent initial cylindrical holes from touching, yet allows the adjacent surface-transformed spheres to combine and form pipe and plate empty spaces, as shown in Figures 11A-11C and Figures 12A-12B and described below.

Figures 11A-11C illustrate a process to form a wafer with a pipe-shaped empty space, according to various embodiments of the present subject matter. A linear array of cylindrical holes 1121 is formed in a surface 1122 of a solid substrate 1119. The cylindrical holes 1121 have a center-to-center spacing (D_{NT}) as calculated using Equation No. 14. The substrate 1119 is heated (annealed) and undergoes the transformation illustrated in Figures 11B through 11C. The result of the surface transformation process is an empty pipe-shaped void 1124 formed below the surface 1122 of the substrate 1119. The radius (R_P) of the pipe 1124 is provided by the following equation:

(15) $$R_P = \sqrt{\frac{8.86 \times R_C^{\,3}}{D_{NT}}}.$$

Figures 12A-12B illustrate a process to form a cellular substrate with a plate-shaped empty space, according to various embodiments of the present subject matter. A two-dimensional array of cylindrical holes 1221 is formed in a surface 1222 of a solid substrate 1219. The cylindrical holes 1221 have a center-to-center spacing (D_{NT}) as calculated using Equation No. 14. The material is heated (annealed) and undergoes the transformation illustrated in Figures 12B. The result of the surface transformation process is an empty plate-shaped void 1225 formed below the surface 1222 of the substrate 1219. The thickness (T_P) of a plate 1225 is given by the following equation:

(16) $$T_P = \frac{27.83 \times R_C^{\,3}}{D_{NT}^{\,2}}$$

Various embodiments disclosed herein form a flexible cellular substrate using surface transformation. In various embodiments, the present subject matter forms a precisely-determined arrangement of voids using surface transformation to provide a cellular material with a relationship between stiffness (S) and density (ρ) approaching that of a perfect cellular material ($S \propto \rho \, x \, h^3$). In various embodiments, a precisely-determined arrangement of voids is formed using to provide a substrate with a desired anisotropic stiffness.

The size, shape and spacing of empty spaces is controlled by the diameter, depth and spacing of holes (or trenches) initially formed in a substrate that has a defined melting temperature. Empty spaces or voids are formed after annealing the material in a temperature range below and near the defined melting temperature. The empty spaces or voids are capable of being formed with a spherical shape, a pipe shape, plate shape, various combinations of these shape types, and/or various dimensions for the various shape type and combinations of shape type.

The volume of air incorporated in the surface transformed empty spaces is equal to the volume of air within the initial starting pattern of cylindrical holes. Thus, the surface transformed empty spaces do not cause additional stress in the substrate or a tendency for the substrate to crack.

The surface of the substrate will be smooth after the surface transformed empty spaces are formed if the initial cylinder length (L) is equal to an integer of a critical length (λ_c) such as 1 x λ_c to form one sphere, 2 x λ_c to form two spheres, 3 x λ_c to form three spheres, etc.. If the cylinder length (L) is not equal to an integer of a critical length (λ_c), then the surface of the substrate will have dimples caused by air in the cylinder attributable to the length beyond an integer of a critical length (λ_c). That is, for a given length L and λ_c, the number of spheres formed is the integer of L/λ_c, and the remainder of L/λ_c contributes to the dimples on the surface of the substrate. Dimples formed on the surface can be removed using a polishing process, for example.

Figures 13A-13E illustrate the formation of empty spheres from initial cylindrical holes with the same radii and with varying length. Initial cylindrical holes are represented using dashed lines 1321. These initial cylindrical holes 1321 have the same radius (R_C) and are drilled or otherwise formed to different depths as represented by Figures 13A, 13B, 13C, 13D and 13E. The resulting surface-transformed spheres 1323 are illustrated with a solid line, as are the surface dimples 1326 that form when the cylindrical hole depth is not an integer multiple of λ_C. These surface dimples can be removed using a simple polishing process to leave a smooth surface with uniform and closed spherical voids within the material. The vertical position and number of the spherical voids is determined by the depth of the initial cylindrical holes.

In various embodiments of the present subject matter, the cellular substrate is formed by appropriately spacing the holes such that, upon annealing the material to provide the surface transformation process, the voids are uniformly spaced (or approximately uniformly spaced) throughout the volume of the cellular material. The uniformly spaced voids provide the cellular material with a uniform density from a macroscopic level and a uniform flexibility across a wafer.

In various embodiments, it is desirable to provide a cellular substrate with a very low density within appropriate constraints for the ability to withstand various strain forces. Figure 14 illustrates a wafer with a surface-transformation-formed stack of empty plates with a large filling factor or low density, according to various embodiments of the present invention. For example, the illustrated filling factor is approximately equal to 0.78, which provides a relatively high porosity and a relatively low density. In the illustrated example, the surface transformation produces a vertical stack of empty plates 1424 in the substrate 1419. The number of empty plates formed depends on the length of the holes. From Equation No. 16, it is determined that the thickness T_P of the empty plate has a maximum value of 6.95 x R_C when D_{NT} is near the minimum allowed value of 2 x R_C as inferred from

Equation No. 14. From Equation No. 13, the center-to-center spacing (λ) of empty plates is 8.89 x R_C. It can be calculated that f $\approx$0.78. Thus, it is expected to be able to use surface transformation to form a cellular substrate with a density of less than one fourth that of a solid volume of material.

4. Bond Relaxed Ultra-Thin Semiconductor Membrane with Bowed Shape to Rigid Substrate

Figures 15A-15C illustrate a process for straining a semiconductor layer by performing a bond-cut process to bond a relaxed bow-shaped semiconductor layer to and flatten the semiconductor layer against a rigid substrate, according to various embodiments of the present invention. In various embodiments, an ultra-thin membrane 1503, such as ultra-thin silicon, is bowed when cut from the crystalline sacrificial wafer 1505 and attached to a rigid substrate 1530. One method to achieve this is to polish or otherwise form the single crystal sacrificial wafer 1503 such that the top surface of the crystal has a curved or contoured surface 1531. Thin or ultra-thin slices are cut from the crystal using a bond-cut process, including an ion implant 1506, such as was discussed and illustrated with respect to Figures 5A-5D. In a relaxed free state, these thin membranes 1503 have a bowed shape. The naturally bowed membrane 1503 is flexed to straighten or flatten it, such that intrinsic strain is introduced in this thin membrane. The thin bowed wafer is bonded to a regular flat unstrained wafer 1530. The strain in the resulting strained membrane is controlled by controlling the direction and amount of the curved surface 1531 of the sacrificial wafer 1505.

5. Bond Single Crystal Wafer with Relaxed Concave Surface to Rigid Substrate

Figures 16A-16D illustrate a process for straining a semiconductor layer by bonding a concave surface of a crystalline wafer to a rigid substrate, according to various embodiments of the present invention. In various embodiments, a regular thickness single crystalline wafer 1632 is cut or otherwise provided with a concave surface 1633. This wafer 1632 is also under strain when straightened and bonded to a regular thickness unstrained wafer 1630, such as a silicon wafer. In various embodiments, the strained wafer 1632 is further thinned after bonding to control the strain.

6. Methods of Straining a Semiconductor Layer at a Wafer Scale

Figure 17 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the present invention. At 1740, a predetermined bowed contour is formed in a flexible one of a wafer-sized semiconductor membrane and a substrate wafer. The wafer-sized semiconductor membrane is bonded to the substrate wafer and the predetermined bowed contour is straightened at 1741. The illustrated process performed at 1741 can occur in a single or in separate steps.

Figure 18 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17. At 1840, which generally corresponds to 1740 in Figure 17, a force is applied to bow a flexible substrate wafer. At 1841, which generally corresponds to 1741 in Figure 17, the periphery of a wafer-sized semiconductor membrane is bonded to the periphery of the substrate wafer 1842, and the force is removed to allow the flexible substrate wafer to straighten 1843. A slight bow may remain in the flexible substrate due to the strain in the semiconductor membrane.

Figure 19 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in

Figure 17. At 1940, which generally corresponds to 1740 in Figure 17, a force is applied to bow a flexible substrate wafer. At 1941, which generally corresponds to 1741 in Figure 17, the periphery of a wafer-sized semiconductor membrane is bonded to the periphery of the substrate wafer 1942, the force is removed to allow the flexible substrate wafer to straighten 1943, and the composite of the membrane and thin substrate is bonded to a thicker carrier substrate 1944. A slight bow may remain in the flexible substrate due to the strain in the semiconductor membrane.

Figure 20 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17. At 2040, which generally corresponds to 1740 in Figure 17, a predetermined bowed contour is formed in a flexible wafer-sized semiconductor membrane. At 2041, which generally corresponds to 1741 in Figure 17, the wafer-sized semiconductor membrane is bonded to the substrate wafer and the bowed contour is straighten. The bonding and straightening can occur as a single or as multiple steps. A slight bow may remain in the flexible substrate due to the strain in the semiconductor membrane.

Figure 21 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in Figure 17. At 2140, which generally corresponds to 2040 in Figure 20, a surface of a sacrificial crystalline wafer is polished such that the surface has a predetermined convex contour. At 2141, which generally corresponds to 2041 in Figure 20, a bond cut process is performed to form and bond an ultra-thin membrane to the substrate wafer. In a relaxed state, the ultra-thin membrane has a convex shape attributable to the polished surface of the sacrificial crystalline wafer. The bonded ultra-thin membrane is flattened, and thus is strained. A slight bow may remain in the flexible substrate due to the strain in the semiconductor membrane.

Figure 22 illustrates a process for forming a wafer with a strained semiconductor layer, according to various embodiments of the process illustrated in

Figure 17. At 2240, which generally corresponds to 2040 in Figure 20, a crystalline wafer is polished, cut or otherwise processed to provide a crystalline wafer with a concave surface. At 2241, which generally corresponds to 2041 in Figure 20, the concave surface of the crystalline wafer is bonded to the substrate wafer such that the bonding flattens and strains the membrane. At 2245, the bonded crystalline wafer is polished to thin the bond wafer and control the strain induced in the membrane.

7. Transistor

Figure 23 illustrates a transistor fabricated with a strained semiconductor membrane, according to various embodiments of the present invention. The illustrated transistor 2350 includes a crystalline semiconductor substrate 2351, and a crystalline semiconductor membrane 2352 bonded to the substrate 2351 with a desired strain in accordance with this disclosure. A gate dielectric 2353 is formed on the strained membrane, and a gate 2354 is formed on the gate dielectric 2353. First and second diffusion regions 2355 and 2356 are formed. The strained semiconductor membrane 2352 between the first and second diffusion regions 2355 and 2356 forms a channel region 2357.

8. Systems

Figure 24 is a simplified block diagram of a high-level organization of a memory device according to various embodiments of the present invention. The illustrated memory device 2460 includes a memory array 2461 and read/write control circuitry 2462 to perform operations on the memory array via communication line(s) 2463. The illustrated memory device 2460 may be a memory card or a memory module such as a single inline memory module (SIMM) and dual inline memory module (DIMM).

The memory array 2461 includes a number of memory cells 2464. The memory cells in the array are arranged in rows and columns. In various embodiments, word lines 2465 connect the memory cells in the rows, and bit lines 2466 connect the memory cells in the columns. The read/write control circuitry 2462 includes word line select circuitry 2467, which functions to select a desired row. The read/write control circuitry 2462 further includes bit line select circuitry 2468, which functions to select a desired column.

Figure 25 illustrates a simplified block diagram of a high-level organization of an electronic system according to various embodiments of the present invention. In various embodiments, the system 2570 is a computer system, a process control system or other system that employs a processor and associated memory. The electronic system 2570 has functional elements, including a processor or arithmetic/logic unit (ALU) 2571, a control unit 2572, a memory device unit 2573 (such as illustrated in Figure 24) and an input/output (I/O) device 2574. Generally such an electronic system 2570 will have a native set of instructions that specify operations to be performed on data by the processor 2571 and other interactions between the processor 2571, the memory device unit 2573 and the I/O devices 2574. The control unit 2572 coordinates all operations of the processor 2571, the memory device 2573 and the I/O devices 2574 by continuously cycling through a set of operations that cause instructions to be fetched from the memory device 2573 and executed. According to various embodiments, the memory device 2573 includes, but is not limited to, random access memory (RAM) devices, read-only memory (ROM) devices, and peripheral devices such as a floppy disk drive and a compact disk CD-ROM drive. As one of ordinary skill in the art will understand, upon reading and comprehending this disclosure, any of the illustrated electrical components are capable of being fabricated on wafers with a full wafer-bonded, mechanically strained semiconductor layer, in accordance with various embodiments of the present invention.

The illustration of the system 2570 is intended to provide a general understanding of one application for the structure and circuitry, and is not intended to serve as a complete description of all the elements and features of an electronic system according to the various embodiments of the present invention. As one of ordinary skill in the art will understand, such an electronic system can be fabricated in single-package processing units, or even on a single semiconductor chip, in order to reduce the communication time between the processor and the memory device.

Applications containing memory cells as described in this disclosure include electronic systems for use in memory modules, device drivers, power modules, communication modems, processor modules, and application-specific modules, and may include multilayer, multichip modules. Such circuitry can further be a subcomponent of a variety of electronic systems.

CONCLUSION

Various embodiments disclosed herein provide strained semiconductor layers by mechanically stretching a semiconductor layer during full wafer-bonding. This disclosure includes several processes, circuit diagrams, and structures. The present invention is not limited to a particular process order or logical arrangement. Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement which is calculated to achieve the same purpose may be substituted for the specific embodiments shown. This application is intended to cover adaptations or variations. It is to be understood that the above description is intended to be illustrative, and not restrictive. Combinations of the above embodiments, and other embodiments, will be apparent to those of skill in the art upon reviewing the above description. The scope of the present invention should be determined with reference to the appended claims, along with the full scope of equivalents to which such claims are entitled.